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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,367	06/15/2001	Isik C. Kizilyalli	41277/MJM/A717	6713

23363 7590 09/13/2002

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EXAMINER

GUERRERO, MARIA F

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 09/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/882,367

Applicant(s)

KIZILYALLI ET AL.

Examiner

Maria Guerrero

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.

- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is the First Action on the merits.

Claims 1-26 are pending.

Information Disclosure Statement

2. The Examiner has considered the information disclosure statement (IDS) filed on June 15, 2001. A copy is attached it.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 13, and 17 recites the limitation "formed one of on and in said substrate". This limitation renders the claim vague and indefinite.

Claim 17 recites the limitation "said associated isolation structure" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim 24 recites the limitation " said amorphous silicon film " in lines 9-12. There is insufficient antecedent basis for this limitation in the claim.

Claim 26 recites the limitations "said dielectric film", "said amorphous silicon film" in lines 4-5. There is insufficient antecedent basis for these limitations in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6, 10-15, 17-22, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. 6,399,450) in view of Shiozawa et al. (U.S. 5,970,352).

Yu discloses a process for manufacturing a semiconductor transistor having elevated (raised) source and drain regions (abstract). Yu teaches providing a transistor gate 18 on a substrate surface and a source/drain region (22/24) defined as surface region extending laterally from the transistor gate 18 (Fig. 2). Yu teaches forming an amorphous silicon layer 53 including a dopant, converting the amorphous silicon layer 53 to a single crystalline silicon layer by using an excimer laser annealing process, the annealing process is controlled so that layer 53 is fully melted and substrate 14 is not melted (selective laser annealing) (col. 6, lines 45-60).

In addition, Yu shows forming an insulating layer over the raised source/drain contact structure and utilizing conventional MOSFET fabrication processes to form contacts (Fig. 1, column 7, lines 6-12)

Furthermore, Yu teaches providing a semiconductor substrate having a surface, providing a transistor region in the substrate, forming a gate stack including a gate electrode 36 formed over a gate dielectric 34 (Fig. 2, col. 3, lines 63-67, col. 4, lines 3-

10, 37-40). Yu discloses the gate stack is covering with an insulating material, the lateral portions of the transistor region not covered by the gate stack being designated source/drain regions (col. 5, lines 17-45). Yu teaches forming a discrete amorphous silicon layer 53 including dopant impurities over the transistor region, irradiating with a laser beam, removing the energy associated with the annealing process (allowing cooling) to convert the discrete amorphous silicon layer 53 to a crystalline silicon layer, and activating the dopant impurities in the source/drain regions (Fig. 7-8, col. 6, lines 10-30, 47-65). Yu discloses forming the opposed duality of discrete raised source/drain contact structures (Fig. 1 and 8).

Furthermore, Yu teaches forming a dielectric structure over the gate stack prior the step of forming the discrete amorphous silicon film, portions of the dielectric structure cover (encroach) the sides of the gate stack, and forming the amorphous silicon film over at least portions of the dielectric structure (Fig. 3-5, col. 5, lines 40-60).

5. Regarding claims 1, 17, and 24, Yu fails to show patterning the crystalline silicon layer to form a duality of raised source/drain contact structures, implanting impurities into the crystalline silicon layer and the source/drain region after the step of converting. However, Yu teaches the patterning the amorphous layer to form the duality of raised source/drain contact structures (Fig. 4-6, col. 5, lines 64-67, col. 6, lines 1-15), implanting impurities prior to the step of converting. However, a person of ordinary skill in the art would recognize that selection of any order of performing process steps is prima facie obvious in absence of new or unexpected results. Ex parte Rubin, 128 USPQ 440 (Bd. APP. 1959). See also In re Burhans, 154 F.2d 690, 69 USPQ 330

(CCPA 1946). Furthermore, Shiozawa et al. shows patterning the crystalline silicon film to form interconnections over the source/drain regions and implanting impurities into the crystalline silicon layer and the source/drain region (Fig. 3(f)-3(h), col. 6, lines 15-35).

6. Regarding claims 1-6, 10-15, 17-22, 24-26, Yu fails to show the substrate having isolation structures, patterning the crystalline silicon layer to form a duality of raised source/drain contact structures that extend over at least part of the isolation structures, converting the amorphous silicon layer to a polycrystalline silicon layer. However, Shiozawa et al. shows forming isolation structures on the semiconductor substrate, providing the transistor comprising a metal gate, and patterning the crystalline silicon film to form interconnections over the source/drain regions and extending on to the isolation regions (Fig. 3(a)-3(c), 3(f)-3(g), col. 3, lines 62-67, col. 4, lines 1-10, 22-40, col. 6, lines 15-25, 60-65). Shiozawa et al. also teaches converting the amorphous silicon layer to polysilicon (polycrystalline silicon), forming the insulating layer over the raised source/drain contact structures, and forming at least one contact opening through the insulating layer to expose a corresponding portion of the raised source/drain contact structures (Fig. 3(j), col. 5, lines 25-30, col. 6, lines 35-40).

7. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Yu's process by including the teaching of Shiozawa et al. The modification would complete an integrated circuit structure having isolation structures that would define the active area, would increase planarity, and would increase the alignment margin for forming contacts to the elevated source and drain regions (Shiozawa et al., col. 4, lines 24-40, col. 6, lines 60-65).

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8. Claims 7-9, 16, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. 6,399,450) and Shiozawa et al. (U.S. 5,970,352) as applied to claims 1-3, 5-6, 9, 11-22, 24-26 above, and further in view of Kohno et al.

Regarding claim 9, Yu fails to show the transistor gate including a metal gate and the step of converting does not melt the metal gate. However, Shiozawa et al. teaches providing the transistor comprising a metal gate (col. 4, lines 50-65). Shiozawa et al. does not show the metal gate being melted. Therefore, a person of ordinary skill would recognize that the metal gate would not be melted during Yu's converting process because only the amorphous silicon layer is melted.

Regarding claims 7-9, 16, and 23, the combination of Yu and Shiozawa et al. fail to show using an XeCl excimer laser emitting light, the excimer laser emits radiation at or near the absorption peak of silicon. However, Kohno et al. shows a crystallization process using the XeCl excimer laser emitting light (308 nm) and the excimer laser energy emitting radiation that is almost absorbed in silicon (near the absorption peak of silicon) (page 252).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Yu and Shiozawa et al. by specifying the use of XeCl excimer laser as taught Kohno et al. because the wavelength corresponded with the wavelength utilized by Yu (308 nm) (Yu, col. 6, lines 46-48). The modification would reduce the time for crystallization (Kohno et al., page 252).

Conclusion


9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tsukamoto (U.S. 5,401,666) shows XeCl excimer laser annealing for activating a source/drain region. Moslehi (U.S. 5,496,750) shows forming elevated source/drain structures. Yu (U.S. 6,372,584) teaches a method for making raised source/drain regions using laser. Robert C. Weast "CRC Handbook of Chemistry and Physics" is cited to show that the absorption peak is a wavelength of maximum electromagnetic absorption (F-73-F-74).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 703-305-0162.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


Maria Guerrero
Patent Examiner
September 9, 2002